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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/551,962	04/19/2000	Henry Esmond Butterworth	GB9-1999-0117US1	3838

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EXAMINER	
CHANG, JUNGWON	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 07/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/551,962	BUTTERWORTH ET AL.
	Examiner	Art Unit
	Jungwon Chang	2154

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 are presented for examination.

2. In view of the appeal brief filed on 4/19/04, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The claim language in the following claims is not clearly understood.

i. As to claim 1, line 3, it is not clearly understood what is meant by "while the slave memory accesses the memory" (i.e., while the slave processor accesses the memory).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faucon et al. (US 6,442,671), hereinafter Faucon, in view of Datta et al. (US 6,393,572), hereinafter Datta.

7. As to claims 1 and 4, Faucon discloses the invention substantially as claimed, including a data processing system allowing a master processor (101, fig. 1) to access a memory (130, fig. 1) by using a slave processor (120, fig. 1) to access the memory (i.e., transfer data between DSP (master processor), and memory via coprocessor (slave processor); col. 6, lines 41-44) and write the data from memory to the master processor (i.e., transfer data between a DSP (master processor), and a memory; col. 2, lines 22-31 and 35-41; col. 5, lines 35-37; write transaction from DSP (master processor) to

memory; col. 5, lines 56-62) comprising:

a master processor (101, fig. 1);

a slave processor (120, fig. 1);

a memory (130, fig. 1); and

a bus subsystem (105, 110, fig. 1) interconnecting the master processor, the slave processor, and the memory (col. 4, line 66 – col. 5, line 9; col. 5, lines 21-25);

wherein the master processor is configured to generate (i.e., DSP (master processor), generating an address in memory; col. 6, lines 15-25 and 32-36), in response to a memory access instruction (i.e., read or write), a read request comprising a read command for execution by the slave processor to read data stored in a location in the memory specified by the memory access instruction (i.e., read transaction (ext0 read) from memory; col. 5, line 66 – col. 6, line 5; transfer data between DSP (master processor), and external memory via coprocessor (slave processor); col. 6, lines 41-44; read transaction (read_mem) from memory; col. 8, lines 63-65) and writes the data from memory to the master processor (i.e., data transfer from memory to DSP (master processor); col. 8, line 66 – col. 9, line 4), and to write the read request to the slave processor (245, 280, fig. 2) via the bus subsystem (i.e., PESRCN bus, 252b, fig. 2, is coupled to latch 245, fig. 2 and ext0 decoder, 280, fig. 2 (slave processor); col. 5, lines 65 – col. 6, line 5), and the slave processor (245, 280, fig. 2) is configured to execute the read command received in the read request from the master processor to obtain the data stored at the specified location in the memory (i.e., read transaction (ext0 read) from memory; col. 6, line 7-8; read transaction (read_mem) from memory;

col. 8, lines 63-65) and to write the data obtained to the master processor via the bus subsystem (i.e., bus, 255a, fig. 2 (mem_out) takes the data from memory, and the data is transferred to DSP (master processor); col. 8, line 66 – col. 9, line 4).

8. Faucon does not specifically disclose while the master processor continues other processing tasks while the slave processor accesses the memory. However, Datta discloses while the master processor continues other processing tasks while the slave processor accesses the memory (i.e., coprocessor (slave processor) is used to off-load tasks from the main processor (master processor) to allow the main processor (master processor) to perform other tasks while the coprocessor (slave processor) simultaneously performing the offloaded tasks; col. 1, lines 11-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Faucon and Datta because Datta's allowing the master processor to continue other processing tasks while the slave processor accesses the memory would reduce the workload on master processor of Faucon's system by distributing tasks of the master processor to other processor.

9. As to claim 2, Faucon discloses the bus subsystem comprises two buses interconnected by a bridge device and the slave processor is integrated in the bridge device. Faucon discloses interconnected two buses (i.e., 250a, 255c, fig. 2) are used for transferring data between master processor and memory (col. 5, lines 53-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made

to include bridge device in Faucon's system because bridge is a device positioned on a bus that allows additional bus to be interconnected with the bus on the bridge is well known in the art at the time the invention was made.

10. As to claim 3, it is rejected for the same reasons set forth in claims 1 and 4 above. Faucon discloses that processor (101, fig. 1) or coprocessor (120, fig. 1) communicates with disk drives (i.e., ROM, RAM, storage device, memory; 102-104, 130, fig. 1). However, Faucon does not specifically use a term disk controller. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include disk controller in Faucon's system because disk controller is a circuit that allows the processor to communicate with a hard disk, floppy disk or other kind of disk drive is well known in the art at the time the invention was made.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Johnson et al, patent 4,878,166, Pickett, patent 5,940,876, Fujiyama, patent 6,009,493, Fadavi-Ardekani et al, patent 6,263,075, Kawai et al, patent 5,584,010 disclose direct memory access control device and method in multiprocessor system for transferring data.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jungwon Chang whose telephone number is (703)305-9669. The examiner can normally be reached on 9:30-6:00 (Monday-Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (703)305-8498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JWC
July 7, 2004

JOHN FOLLANSBEE
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